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(54) Title: PROGRAMMABLE LOGIC CELL AND ARRAY

(57) Abstract

A programmable logic array (10) comprising cells (22) and a bus network (12) in which the cells are arranged in a two-dimensional matrix of rows and columns and are interconnected by the bus network (12). The cells (22) are also interconnected by a two-dimensional array of direct connections between a cell (22) and its four nearest neighbors, one to its left (or to the West), one to its right (or to the East), one above it (or to the North) and one below it (or to the South). Each cell (22) comprises eight inputs, eiht outputs, means for multiplexing the eight inputs onto two leads and logic means that operate in response to the signals on the two leads to produce output signals which are applied to the eight outputs. The bus network (12) comprises a local (25), a turning (26) and an express bus (27) for each row and column of the array (10) and repeater means (24) for partitioning said buses of a given row or column so as to form bus segments. The bus network (12) provides for transfer of data to the cells (22) of the array (10) without using the cells (22) as individual wires.

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PROGRAMMABLE LOGIC CELL AND ARRAY

Cross Reference to Related Patents and Applications

The following U.S. patents and applications are
related and are incorporated herein by reference: U.S.
5 Patent 4,700,187 for "Programmable Asynchronous Logic
Cell and Array", U.S. Patent 4,918,440 for
"Programmable Logic Cell and Array", Application No.
07/378,106 filed July 11, 1989 for "Programmable Logic
Cell and Array", and Application No. 07/427,160 filed
10 October 25, 1989 for "Programmable Logic Cell and
Array".

Field of the Invention

This invention relates to the field of digital
15 logic circuits and, more particularly, to programmable
and reprogrammable logic devices.

Background of the Invention

U.S. Patent Application No. 07/427,160, describes
20 a two dimensional array of programmable logic cells.
Each of these cells accepts two "A" inputs, one each
from two of its nearest neighbor cells in the array and
two "B" inputs, one each from the other two of its
nearest neighbors. Each cell performs selected
25 operations on one of the "A" inputs and one of the "B"
inputs to generate outputs on two "A" outputs and two
"B" outputs. There are exactly four unique
combinations of inputs to (or outputs from) such cells,
i.e., the "A" inputs can come from the nearest neighbor
30 cells to (1) the North and East, (2) the North and
West, (3) the South and East, or (4) the South and West
and the "B" inputs come from the other two cells. The
four cells having these four combinations of inputs are
35 identified as cells 20A, 20B, 20C and 20D of Figs. 1
and 2A-2D of the '160 application. As discussed in the

'160 application, these four combinations of inputs can
be recorded as four orientations of the cell. The
limitations on the directions from which the inputs are
received and the directions in which the outputs are
5 sent impose severe design limitations on the use of
such cells in an array of cells. If cells of only one
type are used, signal propagation in the array can go
in only one direction in each dimension.
Alternatively, as shown in Fig. 1 of '160 application,
10 the four cell types can be assembled into one array to
provide for signal flow in both directions in both
dimensions. However, this arrangement tends to be
inefficient in its use of cells.

        One object of the present invention is to provide
15 a logic cell for use in a programmable logic array,
wherein each logic cell is functionally identical.

        Another object of the present invention is to
provide a means for transmitting data within the array
by means other than the interconnection of individual
20 logic cells so as to minimize the time required to
transmit data within the array.

Summary of the Invention

        The present invention is an array of programmable
25 logic cells. In a preferred embodiment, each logic
cell has at least eight inputs, eight outputs, means
for multiplexing the eight inputs onto two leads and
logic means that operate in response to the signals on
the two leads and control bits, to produce output
30 signals which are applied to the eight outputs.

        The logic cells of the array are arranged in a
two-dimensional matrix such that each cell has four
nearest-neighbor cells, one to its left (or to the
West), one to its right (or to the East), one above it
35 (or to the North) and one below it (or to the South).

Signal flow is possible in both directions in both
dimensions.

According to the present invention, the logic
cells forming the two-dimensional array are the same.
5 More specifically, in forming the two-dimensional
matrix, the interconnection of every cell with each of
its four neighboring cells is functionally identical.
In each direction, the cell has two inputs and two
outputs which are connected to the two outputs and two
10 inputs of the nearest neighboring cell. Since the
inputs and outputs are functionally identical on each
side of the cell, every cell of the array has the same
orientation.

In addition, the present invention provides a bus
15 network for transmitting digital data within the array
without requiring the individual cells to act as
logical wires. The bus network has three types of
programmable buses: a local bus, a turning bus and an
express bus, whereby one of each bus type is provided
20 for each row and column of the array. According to the
present invention, the three buses of each row and
column of the array are connected to repeaters so as to
form bus segments, which span a plurality of cells. As
a result, the repeaters partition the array into
25 rectangular blocks of cells to form an arrangement that
can be repeated indefinitely.

The array of the present invention also includes
means for distributing independent timing signals to
each column of cells of the basic array and means for
30 transmitting digital data from either the basic array
of cells or the bus network to an input/output port.

Brief Description of the Drawings
These and other objects, features and advantages
35 of the invention may be better understood by referring

to the following detailed description, which should be
read in conjunction with the accompanying drawing in
which:

   Fig. 1 is a schematic illustration of a preferred
embodiment of the invention depicting an exemplary
portion of an array of cells with a bus network
superimposed on the array;

   Fig. 2 is a diagrammatic illustration of an
exemplary portion of the array of cells according to
the present invention;

   Fig. 3 is a block diagram depicting the internal
structure of a cell of Fig. 2;

   Figs. 4A-4D are diagrammatic illustrations of a
set of possible states of a logic means in a cell of
Fig. 3;

   Fig. 5 is a diagrammatic illustration depicting
further details of the bus network superimposed on an
array of cells according to the present invention;

   Fig. 6 is a diagrammatic illustration of the
interconnection scheme between the array of Fig. 2 and
local bus segments of the bus network;

   Fig. 7 is a diagrammatic illustration of the
interconnection scheme between the array of Fig. 2 and
turning bus segments of the bus network;

   Fig. 8 is a diagrammatic illustration of the
interconnection scheme between the array of Fig. 2 and
express bus segments of the bus network;

   Fig. 9 is a diagrammatic illustration of a set of
connections that can be implemented by a repeater of
the bus network;

   Fig. 10 is a block diagram depicting a clock
distribution network according to the present
invention; and

- 5 -

Fig. 11 is a block diagram depicting the interface between the array of the present invention and an input/output port.

5 Detailed Description of the Drawings

Fig. 1 depicts a programmable logic array 10 comprising cells 22 and a bus network 12 formed in accordance with the present invention. Cells 22 are arranged in a two-dimensional matrix of rows and

10 columns and are interconnected by bus network 12 by connections not shown in Fig. 1. The cells are also interconnected by a two-dimensional array of direct connections between a cell and its four nearest neighbors, (i.e., the four cells immediately adjacent

15 to the North, East, South and West). The bus network 12, which comprises repeaters 24 and vertical and horizontal buses 25, 26, 27, provides for the transfer of data within the array 10 without requiring individual cells 22 to act as logical wires.

20 Fig. 2 depicts the direct interconnections within an exemplary portion of the array of cells 22 formed in accordance with the present invention. As is apparent, the cells are arranged in a two dimensional matrix with each cell having four nearest neighbors, one to its

25 left (or to the West), one to its right (or to the East), one above it (or to the North) and one below it (or to the South). Each cell 22 has eight inputs 31a, 32a, 33a, 34a, 31b, 32b, 33b, 34b and eight outputs 41a, 42a, 43a, 44a, 41b, 42b, 43b, 44b. Each cell 22

30 is identical with respect to its direct connections to its four nearest neighbors. To each such neighbor, the cell provides two outputs and from each such neighbor the cell has two inputs. Cell inputs and outputs are divided into two categories "A" and "B", whereby each

35 cell has an A input, an A output, a B input and a B

output connected to each of its four nearest neighbors.
Between adjacent cells, an A input is always connected
to an A output and a B input is always connected to a B
output.

5   In an illustrative embodiment of cell 22 as shown
in Fig. 3, the cell 22 comprises a four-to-one
multiplexer 52, a six-to-one multiplexer 54 and a logic
unit 56. Logic unit 56 can implement any one of a
plurality of operations, such as, a direct wire, a
10 switch, a logical NAND function, an exclusive OR
function, a flip-flop or a logical constant. Each cell
is controlled by eight configuration bits that are
supplied to the cell by control lines (not shown) from
a configuration control (not shown) such as a
15 read/write memory. The configuration bits are used to
specify which inputs are selected by multiplexers 52,
54 and which operation(s) is implemented by the logic
unit. A clock signal is also provided to each cell by
a clock signal line (not shown).

20   The four "A" inputs 31a, 32a, 33a, 34a are applied
to multiplexer 52 and the four "B" inputs 31b, 32b,
33b, 34b are applied to multiplexer 54. As discussed
below, two other inputs are applied to multiplexer 54
from vertical and horizontal lines 25 of the bus
25 network. Multiplexer 52 connects one of the four "A"
inputs to a lead 55a to logic unit 56. Similarly,
multiplexer 54 connects one of the six "B" inputs to a
lead 55b to logic unit 56. Each multiplexer 52, 54 is
controlled separately by two and three configuration
30 bits, respectively, so as to select one of its inputs.
As a result, there are twenty-four possible
combinations of inputs that can be applied to the logic
unit 56 via leads 55a, 55b.

       Logic unit 56 is a two-input, two-output device
35 which selectively implements one of four possible

combinations of operations as specified by two
configuration bits. Logic unit 56 performs the
selected operation on the input signals on leads 55a,
55b so as to generate output signals on leads 57a, 57b.
5   The signal on lead 57a is applied to the "A" outputs
41a, 42a, 43a, 44a and the signal on lead 57b is
applied to the "B" outputs 41b, 42b, 43b, 44b. As
discussed below, the signal on lead 57a can also be
provided to the bus network via driver 86 under control
10 of another configuration bit.

        Preferably, logic unit 56 comprises a NAND gate
61, an XOR gate 63, a flip-flop 65 and two four-to-one
multiplexers 67, 69. The operation of logic unit 56 is
determined by the state of multiplexers 67, 69, which
15 are controlled in tandem via the two configuration
bits. Figs. 4A-D illustrate the four configurations
(or states) in which the logic unit may be placed.
More specifically, Fig. 4A illustrates a first
configuration, wherein the four "A" outputs are
20 logically connected to a single selected "A" input and
the four "B" outputs are logically connected to a
single selected "B" input. Fig. 4B illustrates a
second configuration, wherein the selected "A" input is
logically connected to the four "B" outputs and the
25 selected "B" input is logically connected to the four
"A" outputs. Fig. 4C illustrates a third configuration
in which a logical NAND function and a logical
exclusive OR function are implemented by the logic unit
56. The logical NAND of the selected "A" input and the
30 selected "B" input is provided on the four "A" outputs.
The logical exclusive OR of the selected "A" input and
the selected "B" input is provided on the four "B"
outputs. Finally, Fig. 4D illustrates the
implementation of a D-type flip-flop. In this
35 configuration, the signal on the selected "B" input is

applied to the enable input of the flip-flop to control
whether the flip-flop maintains its previous state or
reads in data supplied via the selected "A" input lead.
The output of the flip-flop is provided on the four "A"
outputs. A logical "1" (or high signal) is provided on
5 the four "B" outputs. As shown in Fig. 10 below, each
D flip-flop also has a clock input which controls the
timing of changes in the state of the flip-flop.

Fig. 5 illustrates the connection of the bus
network of the present invention to the cells of the
10 array 10 (the direct connections between the cells have
been omitted for clarity). One local bus 25, one
turning bus 26 and one express bus 27 are provided for
each row and each column of the array.

Repeaters 24 partition each bus into bus segments.
15 Each bus of a given row or column of the array is
connected to a repeater 24 at every "n" consecutive
cells with the result that the array is partitioned
into n x n blocks of cells 22. For example, as shown
in Figs. 1 and 5, repeaters 24 are positioned so as to
20 span eight consecutive cells 22, thereby forming an 8 x
8 block of cells. As suggested in Fig. 5, this
arrangement is repeated indefinitely to form arrays of
whatever size is desired. Note, however, that the
direct connections illustrated in Fig. 2 are continuous
25 throughout the array and are not disrupted by the
repeaters or the bus network.

Fig. 6 depicts the interconnection between cells
22 and the local buses of the bus network for an 8 x 8
block of cells. As shown in Fig. 6, the bus network
30 comprises eight vertical local bus segments 25a - 25h
and eight horizontal bus segments 25i - 25p. Each
local bus segment 25a - 25p spans eight consecutive
cells. As shown in Fig. 6, leads 72, 74 provide inputs
to each cell 22 from its associated horizontal and
35

vertical local bus. However, cell 22 can only transmit
data via a lead 76 to one of the horizontal or vertical
buses depending on the location of the cell 22 within
the array. In particular, a checkerboard pattern is
5 used to determine whether a given cell transmits data
to a horizontal bus or a vertical bus. Thus, if a
given cell 22 transmits data to a horizontal bus, then
the four cells 22 immediately adjacent to that cell,
transmit data to the vertical local bus, and
10 vice versa. Illustratively, the cell 22 in the upper
left corner of the array transmits data to its
associated horizontal local bus; and the other cells
alternate their connections in the checkerboard
pattern.

15   As shown in Fig. 3, leads 72, 74 from the
horizontal and vertical buses are connected to each
cell 22 through a horizontal local bus input 82 and a
vertical local bus input 84 of the six-to-one
multiplexer 54. Data is transmitted from the cell to
20 the local bus segment by means of driver 86, which is
connected to the "A" output of each cell 22.

        Driver 86 is controlled via two input lines 88, 89
to provide a tri-state or open-collector function. The
tri-state function, which is independently programmable
25 for each cell via a configuration bit, allows driver 86
to be electrically disconnected from the local bus when
the cell is not used to transmit to the local bus.

        The open-collector function indicates to a
particular cell whether any other cells are currently
30 driving the same local bus segment. In the event a
local bus segment is unused (i.e., no drivers are
transmitting to the local bus segment), the open-
collector capability is turned on and the local bus
segment is pulled high through a passive pull-up
35 resistor. Thus, any unused local bus segment provides

a logical "1" to any cell reading the bus segment. If
only one cell is transmitting to a given local bus
segment, the open-collector function of driver 86 of
all cells capable of driving that bus.segment is off,
5 and the driver of the transmitting cell can output
either an active "1" or active "0". If more than one
cell is driving the same local bus segment, the open-
collector function of the drivers of all the cells
capable of driving that bus segment are turned on to
10 provide a wired-AND function. More specifically, if
any one of the outputs of the cells driving the local
bus segment is a logical "0", then the bus segment is
pulled low, thereby providing a logical "0" to any cell
reading the bus segment.

15   Fig. 7 depicts the connection scheme for the
turning buses of the bus network for an 8 x 8 block of
cells 22. These buses provide connections between the
horizontal and vertical buses. Similar to the local
bus segments there are sixteen turning bus segments 26a
20 - 26p associated with an 8 x 8 block of cells, eight
turning bus segments 26a - 26h running vertically and
eight turning bus segments 26i - 26p running
horizontally. Each turning bus segment traverses eight
orthogonal turning bus segments for an 8 x 8 block of
25 cells and is connected to the eight orthogonal turning
bus segments through a programmable connection that is
schematically represented by the circle 87 at the
intersection of each pair of orthogonal bus segments.
Illustratively, the connection can be effected by a
30 pass transistor controlled by a configuration bit that
is provided to the transistor by a control signal line
(not shown) from a configuration control (not shown).
These connections allow data transmitted on a
horizontal bus to be routed to a bus transmitting data
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in the vertical direction, and _vice versa_, thereby
providing for 90° turns within the bus network.

Fig. 8 illustrates the connection scheme for the
express buses of the bus network for an 8 x 8 block of
5 cells 22. As was the case for the local and turning
bus segments, there are 16 express bus segments 27a -
27p for an 8 x 8 block of cells. However, unlike the
local or turning bus segments, the express bus segments
are connected solely to the repeaters 24. Thus, an
10 express bus segment is the fastest means provided for
transmitting data between two repeaters of a given row
or column.

Repeaters 24 connect the bus segments of one n x n
block of cells to the bus segments of the adjacent n x
15 n block of cells. Each repeater 24 is programmable so
as to allow any one of the three bus segments connected
to ports on one side of the repeater to be connected to
any one of the three bus segments connected to ports on
the other side of the repeater. Thus, each repeater
20 has the functionality of a 3 x 3 crossbar switch. In
particular, a bus segment connected to one side of the
repeater has four connection options with the opposite
side of the repeater. For example, a local bus segment
connected to one side of a repeater can be connected to
25 either the local bus, the turn bus, or the express bus
connected to the other side, or it can be terminated
(i.e. the local bus connected to one side of the
repeater is not connected to any bus on the other
side).

30   Fig. 9 illustrates the various connections that
can be made between the ports of the repeater. As will
be appreciated by those skilled in the art, numerous
devices can be used to implement such connections and
numerous other connection arrangements are possible.
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Another function of each repeater is to provide
signal regeneration. Illustratively, this is
accomplished by providing a driver for each bus line.
As a result, each repeater connection is
5 unidirectional. Advantageously, the direction of
signal flow for each repeater connection is
programmable.

The array of the present invention also provides a
clock distribution network for the distribution of
10 clock signals to the D-type flip-flops 65 in the cells
22 of the array. The clock distribution network is
partitioned by column so as to provide independent
timing signals to each column of cells of the array.
Fig. 10 depicts a clock distribution network comprising
15 one multiplexer 90 for each column of the basic array.
Each multiplexer 90 has four inputs and one output.
The four inputs to the multiplexer are: an external
clock, a logical constant, the express bus adjacent to
the clock distribution network and the "A" output of
20 the cell at the head of the column. The output of the
multiplexer of a given column provides the clock signal
to D-type flip-flop 65 of each cell 22 of the given
column.

In response to two configuration bits, each
25 multiplexer selects a signal from one of its four
inputs and provides such signal as a clock signal to
each cell in its column. The external clock input
allows an external timing signal to be connected to any
or all the columns of the array. The logical constant
30 input can be used to provide a logical "0" to columns
containing no registers so as to reduce power
dissipation. The express bus input can provide a
secondary clock to multiple columns when the external
clock line is used as a primary clock. The fourth
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input, the "A" output, can provide a clock signal to a
single column of cells.

Fig. 11 is a block diagram of the interface
between the array and an input/output-port 92,
hereinafter referred to as an I/O pad. According to
the present invention, for each I/O pad 92 the
interface comprises an input buffer 94, an output
buffer 96, a four-input multiplexer 98 and two
two-input multiplexers 100, 102. Additionally, there
are two adjacent cells 22 on the perimeter of the basic
array dedicated to each I/O pad, one cell being
dedicated as the "input" cell 93 and the other as the
"output" cell 95.

As shown in Fig. 11, the output buffer 96 and
input buffer 94 are both connected to the I/O pad 92.
The input buffer 94 drives the input cell 93 through
the edge-facing "A" input of the input cell. The edge-
facing "A" output of the output cell 95 is connected to
the output buffer 96 via two-to-one multiplexer 102.

The interface logic is controlled via programmable
configuration bits. For example, the threshold level
of the input buffer 94 is selectable to either TTL or
CMOS and the slew rate of the output buffer is
variable. Other selectable functions include an open-
collector function on the output buffer, the enabling
of a pull-up transistor on the I/O pad to prevent
unused I/O pads from floating, and a global override so
as to tri-state all output buffers at power up.

The output buffer 96 is programmable to one of two
states: a "CONFIGURE" mode or a "RUN" mode. In the
CONFIGURE mode, a control signal providing
configuration data is connected to the output buffer 96
via multiplexer 102 and a control signal is connected
to the tri-state function of output buffer 96 via
multiplexer 100. In the RUN mode, the A output of the

output cell 95 is connected to the output buffer 96 via
multiplexer 102 and a control signal is connected to
the tri-state function of the output buffer 96 via
multiplexers 98, 100.

5   Two configuration bits control multiplexer 98 to
select one of four signals for controlling the tri-
state function of the output buffer 96. One of the
four control signals is a logical "0", which turns the
tri-state function of the output buffer 96 off, thereby
10 allowing the output buffer to transmit to the I/O pad
92 (i.e., I/O pad can function only as an output port).
A second control signal is a logical "1", which turns
the tri-state function of the output buffer 96 on,
thereby electrically disconnecting the output buffer 96
15 from the I/O pad 92 (i.e., I/O pad can function only as
an input port). The third and fourth control signals
are the signals transmitted on the output cell's 95
associated local vertical and horizontal bus. The
signals transmitted on the bus are either a logical
20 high or logical low and function to control the I/O pad
as described above.

Finally, each input cell 93 and each output cell
95 associated with an I/O pad 92 are connected directly
to express buses. As shown in Fig. 11, the edge-facing
25 A input of the output cell 95 and the edge-facing A
output of the input cell 93 are connected to express
buses 104, 106. These buses provide a rapid means of
routing input/output signals into and out of the array.

The logic cells of the present invention make the
30 array especially well-suited for register-intensive,
arithmetic and logic applications. This is
accomplished by the inclusion of a register and a half
adder (XOR and NAND) in the logic unit of each cell.
Any of the basic logic functions can be implemented by
35 interconnecting multiple cells and repetitively

performing the exclusive OR and NAND function. For
example, to produce the logical AND, OR and NOR
functions, each of three cells can be configured to the
state shown in Fig. 4C, in which the "A" output of the
5 first cell provides the logical NAND of the selected
"A" and "B" inputs and the "B" output provides an
exclusive OR function of the "A" and "B" inputs. The
"A" and "B" outputs of the first cell are then applied
to the "A" and "B" inputs of the second cell. The
10 outputs of the second cell are connected to the third
cell in a similar manner. For this interconnection
arrangement, the outputs of the second cell provide an
exclusive NOR function and a NOR function of the input
signals of the first cell and the outputs of the third
15 cell provide an AND function and an OR function of the
inputs of the first cell.

From the foregoing description of the invention,
numerous alterations, modifications and improvements
will be readily apparent. Other connection schemes may
20 be used in conjunction with the bus network. For
example, an additional bus may be incorporated whereby,
every third repeater is connected so as to form a super
express bus. In addition, the cells of the present
invention can be modified so as to implement different
25 operations, or a different number of operations or to
accommodate additional inputs or provide more outputs.
Of particular interest, while the invention has been
described in the context of a two dimensional array of
cells in which connections are provided at each cell
30 with its nearest-neighbor cells in both directions in
two dimensions (i.e., to the North and South, to the
East and West), this connection pattern can also be
extended so as to provide connections to other nearest-
neighbor cells in one or both directions in additional
35 dimensions. In particular, for each additional

dimension, each cell of the two dimensional array has an additional two neighboring cells and therefore must provide for an additional two A inputs and two B inputs, one A and one B input from each cell and an

5 additional two A outputs and two B outputs, one A and one B output to each cell. Finally, although the cells of the preferred embodiment are conceptually located on a plane, it is possible to connect the cell inputs and outputs on one edge of the array to the inputs and

10 outputs of the cells on the opposite edge of the array. For example, in a two dimensional array, connecting the cells on two opposite ends of the array results in an array that can be conceptually viewed as a toroid.

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What is claimed is:

1.   A programmable logic array comprising:
         a plurality of logic cells, wherein each cell
5 except those at the edges of the array has four
nearest-neighbor cells, one to the left (or West), one
to the right (or East), one above (or to the North) and
one below (or to the South) so as to form an array in
which said logic cells are aligned in rows and columns,
10 each cell comprising:
         eight inputs, two from each of its four
nearest neighbors,
         eight outputs, two to each of its four
nearest neighbors,
15   means for storing a plurality of control
bits,
         means for multiplexing the eight inputs onto
first and second input leads, the inputs connected to
said input leads being specified by control bits stored
20 in said storing means, and
         logic means for generating signals on said
outputs in response to signals on said input leads and
control bits stored in said storing means.

25   2.   The apparatus of claim 1 wherein a logic cell
receives two inputs from each nearest-neighbor cell and
provides two outputs to each nearest-neighbor cell.

      3.   The apparatus of claim 1 wherein the inputs
30 and outputs associated with the four nearest-neighbor
cells are functionally equivalent.

      4.   The apparatus of claim 1 wherein the logic
means implements a pair of Boolean logic functions.
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5.   The apparatus of claim 1 wherein the logic means implements an exclusive OR and a NAND function.

6.   The apparatus of claim 1 wherein the logic
5 means implements a flip-flop.

7.   The apparatus of claim 1 wherein the logic means provides a constant logic signal to at least one of the outputs.

10
8.   The apparatus of claim 1 wherein the multiplexing means comprises first and second multiplexers each of which has at least four inputs, each of said four inputs to the first multiplexer
15 coming from a different nearest-neighbor cell and each of said four inputs to the second multiplexer coming from a different one of the same nearest-neighbor cell.

9.   The apparatus of claim 1 wherein the logic
20 means has two output leads, one of which fans out to four of said outputs and the other of which fans out to the other four outputs.

10. The apparatus of claim 1 wherein at least
25 three of said cells are connected in series with the outputs of a first cell connected to the inputs of a second cell and the outputs of said second cell are connected to the inputs of third cell, whereby when each cell provides an exclusive OR and logical NAND
30 function on its outputs in the respect to its inputs the first cell provides at its outputs the exclusive OR and NAND of its inputs, the second cell provides at its outputs the exclusive NOR and NOR of the inputs to the first cell, and the third cell provides at its outputs
35 the AND and the OR of the inputs to the first cell.

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11.   In a two dimensional array of logic cells,
each cell except those at the edges of the array having
four nearest neighbors so as to form rows and columns
of said cells, a bus network for transmitting signals
within the array comprising:
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            a local bus, a turning bus and an express bus
provided for every row and column of the array formed
by said cells,

            repeater means for driving said buses, said
repeater means partitioning said buses of a given row
10
or column so as to form bus segments, each bus segment
spanning a plurality of said logic cells.

12.   The apparatus of claim 11 wherein the
repeater means forming the bus segments are aligned in
15
rows and columns which partition said array of cells
into rectangular blocks of said cells.

13.   The apparatus of claim 11 wherein each local
bus segment is connected to every cell spanned by that
20
bus segment so as to provide an electrical connection
between the cells and the bus network.

14.   The apparatus of claim 11 wherein each
turning bus segment provides an electrical connection
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to all orthogonal bus segments between a row of the
array and a column of the array.

15.   The apparatus of claim 11 wherein the express
bus segment is connected solely to the two repeater
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means forming said express bus segment.

16.   The apparatus of claim 11 wherein the
repeater means is programmable to connect any bus
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connected to one side of the repeater means to any bus
connected to the other side of the repeater.

17.   The apparatus of claim 11 wherein the
repeater means provides electrical signal regeneration
for each programmable connection.

18.   The apparatus of claim 11 wherein the
repeater means is programmable so as to select the
electrical signal direction through the repeater means
for a given bus connection.

19.   A programmable logic array comprising:
a plurality of logic cells, wherein each cell
except those at the edges of the array has four nearest
neighbors, one to the left (or West), one to the right
(or East), one above (or to the North) and one below
(or to the South) so as to form an array in which said
cells are aligned in rows and columns, and
clock distribution means for providing
independent timing signals to said logic cells, said
clock distribution means comprising one multiplexer for
each column of the array, each multiplexer having a
plurality of inputs and one output, said output being
connected to each logic cell in the given column.

20.   The apparatus of claim 19 wherein said
multiplexer in the clock distribution means has four
inputs, a first input to said multiplexer being a
constant logical signal, said second input coming from
an external timing source, said third input coming from
an express bus and said fourth input coming from the
output of a logic cell.

21. The apparatus of claim 19 wherein the timing signal provided to the logic cells of a given column of the array is independent from the timing signal of any other column of the array.

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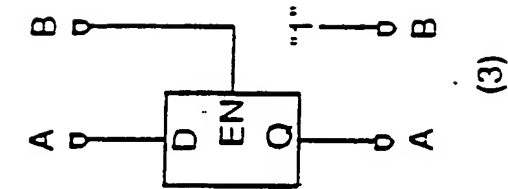25

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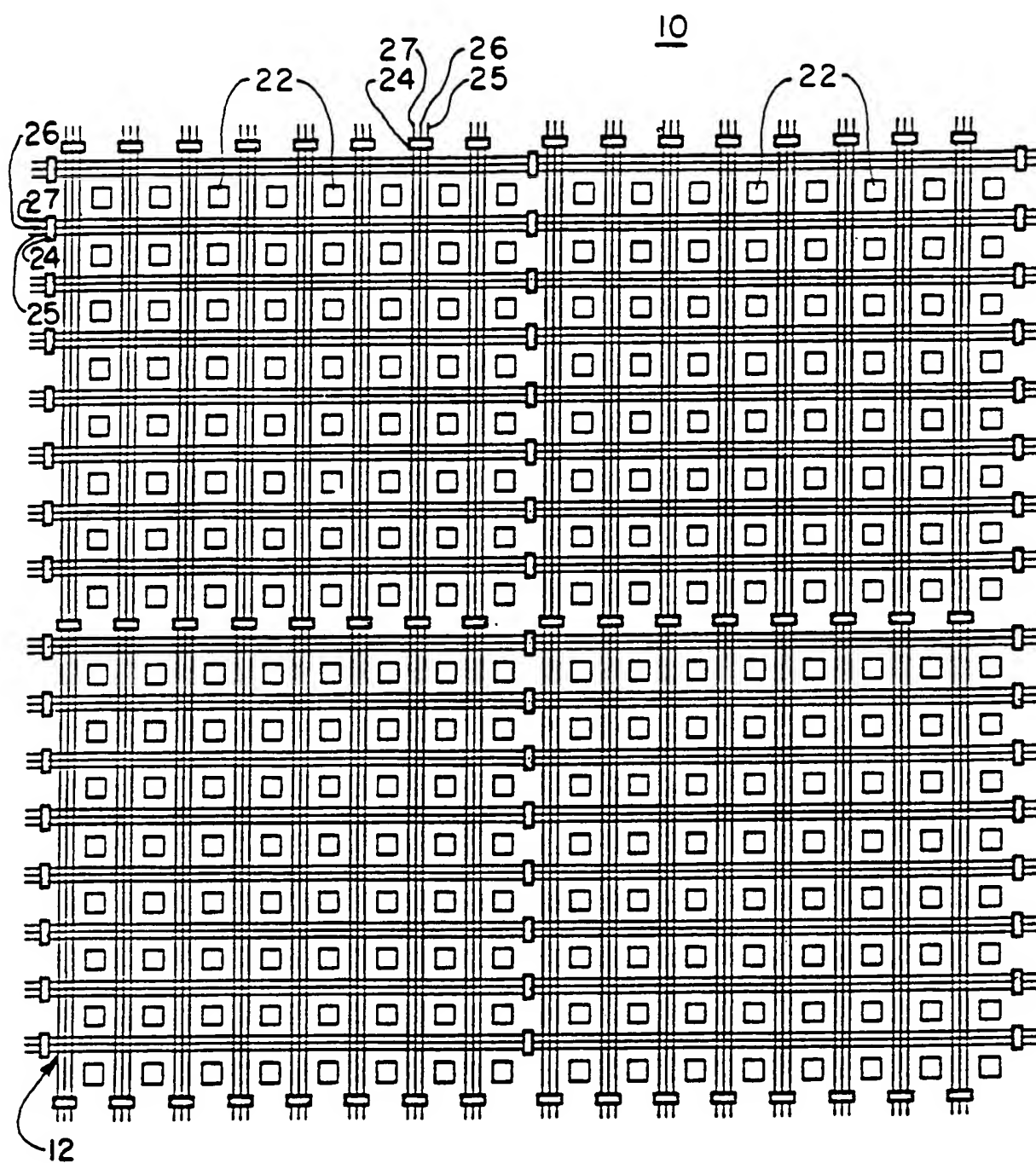
FIG. 1

2/11
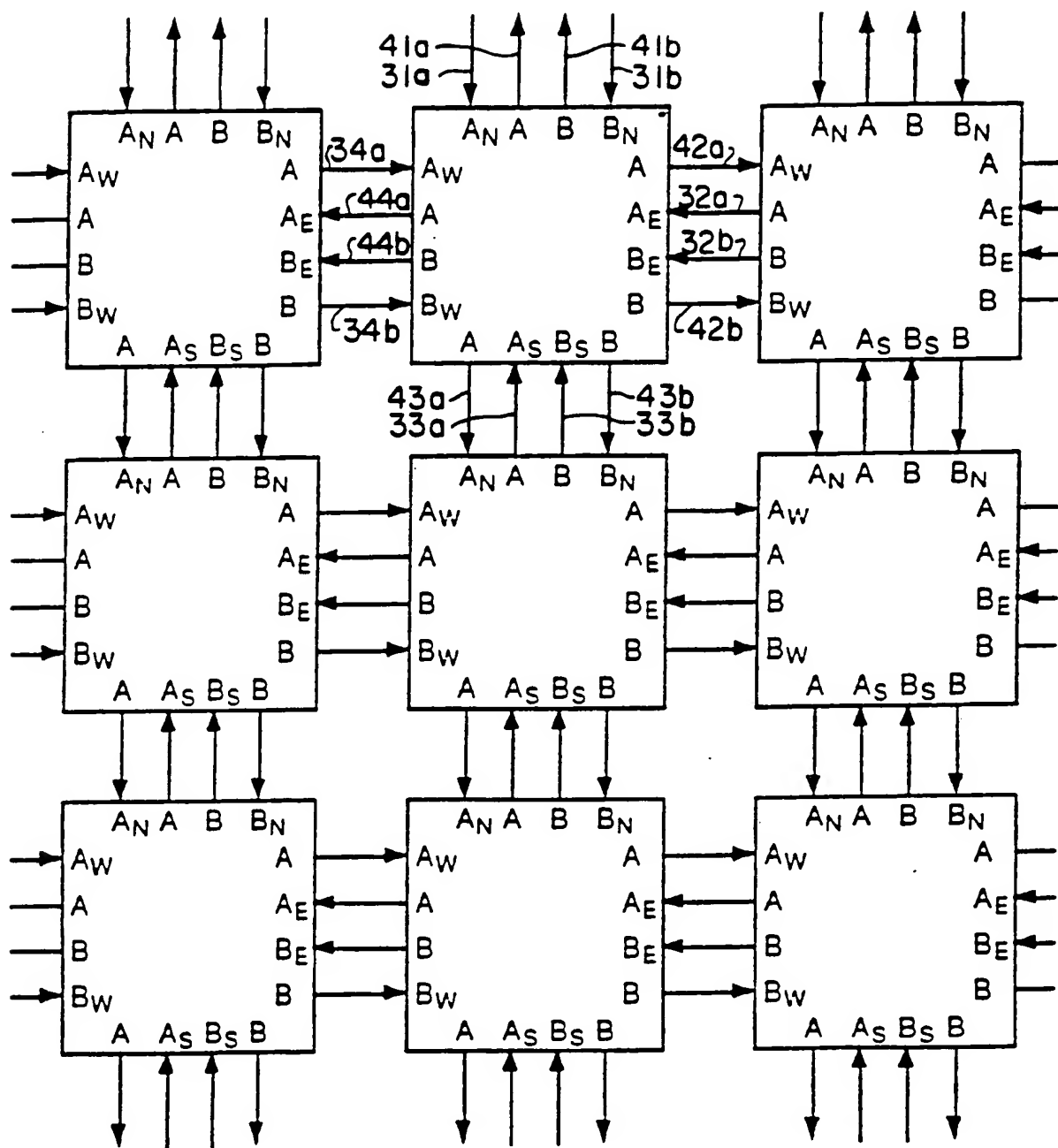
FIG. 2

3/11
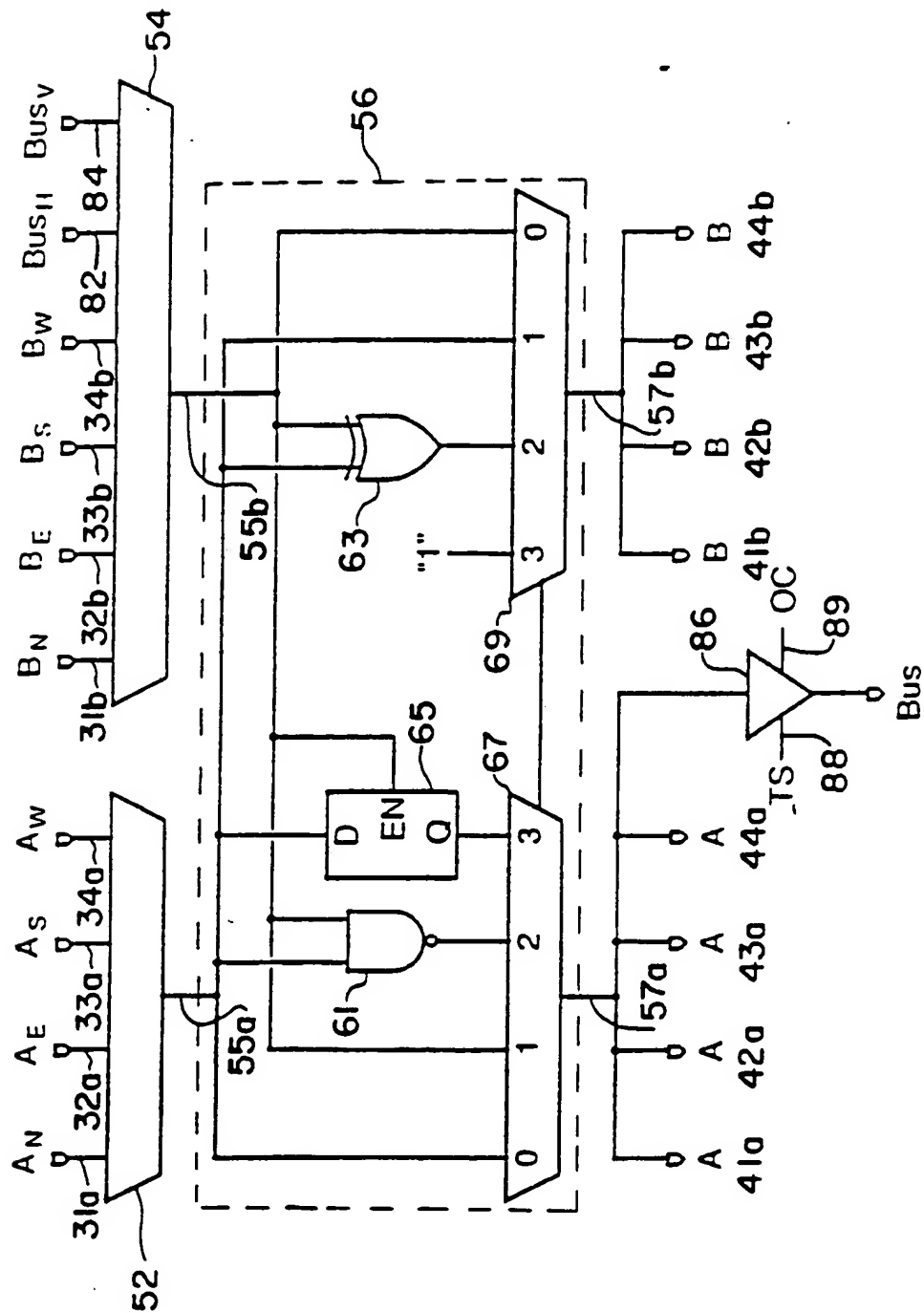
FIG. 3

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FIG.4A (0)

FIG.4B (1)

FIG.4C (2)

FIG.4D (3)

FIG. 5

FIG. 6

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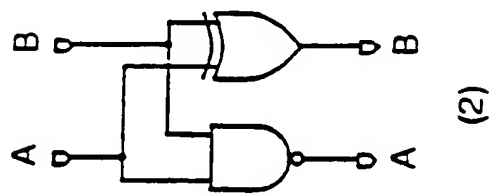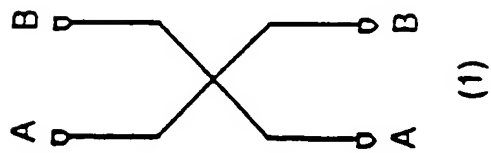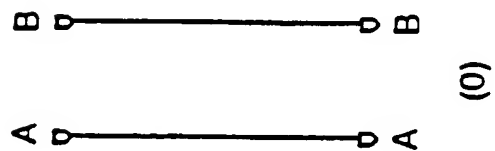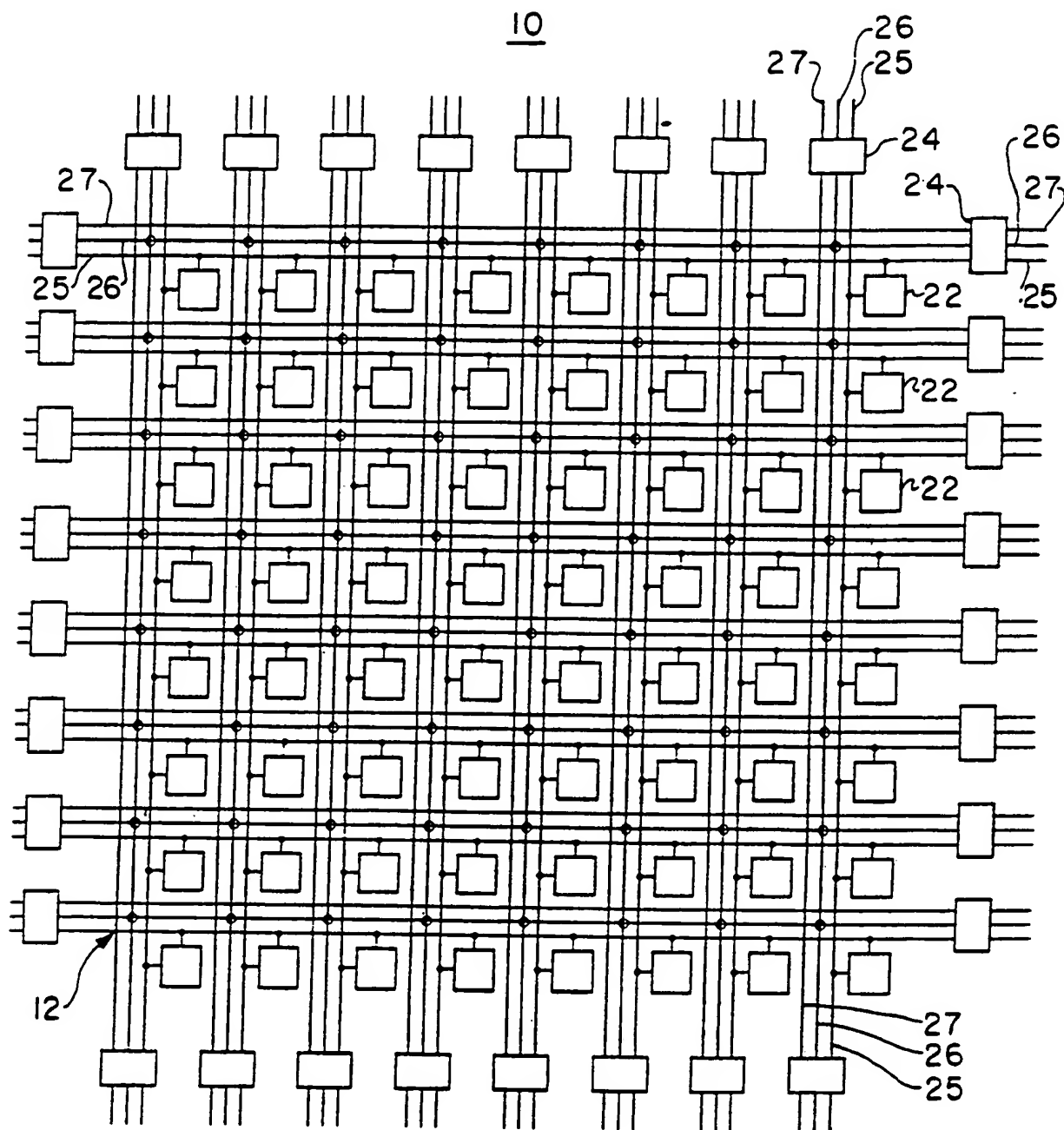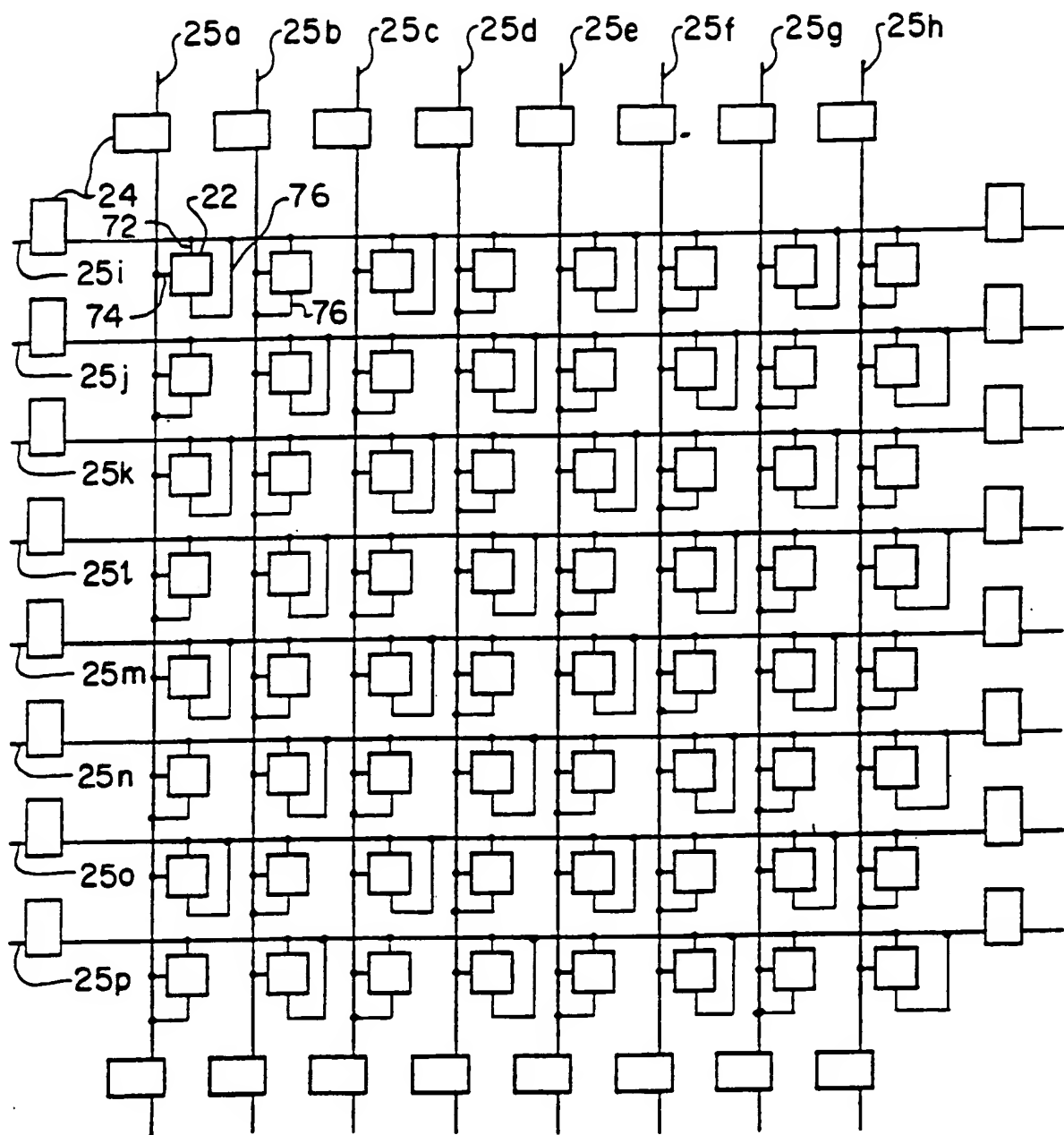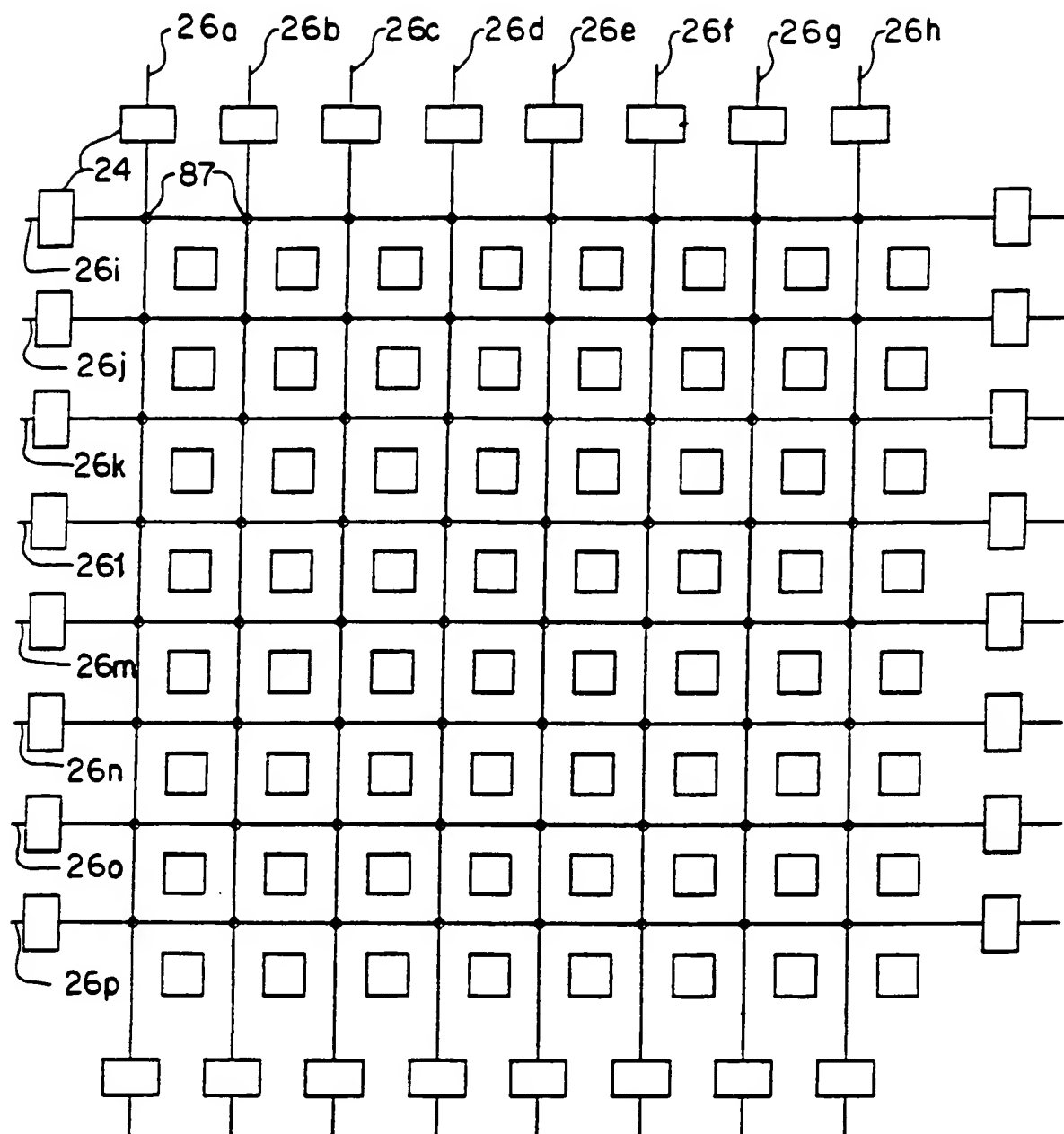
FIG. 7
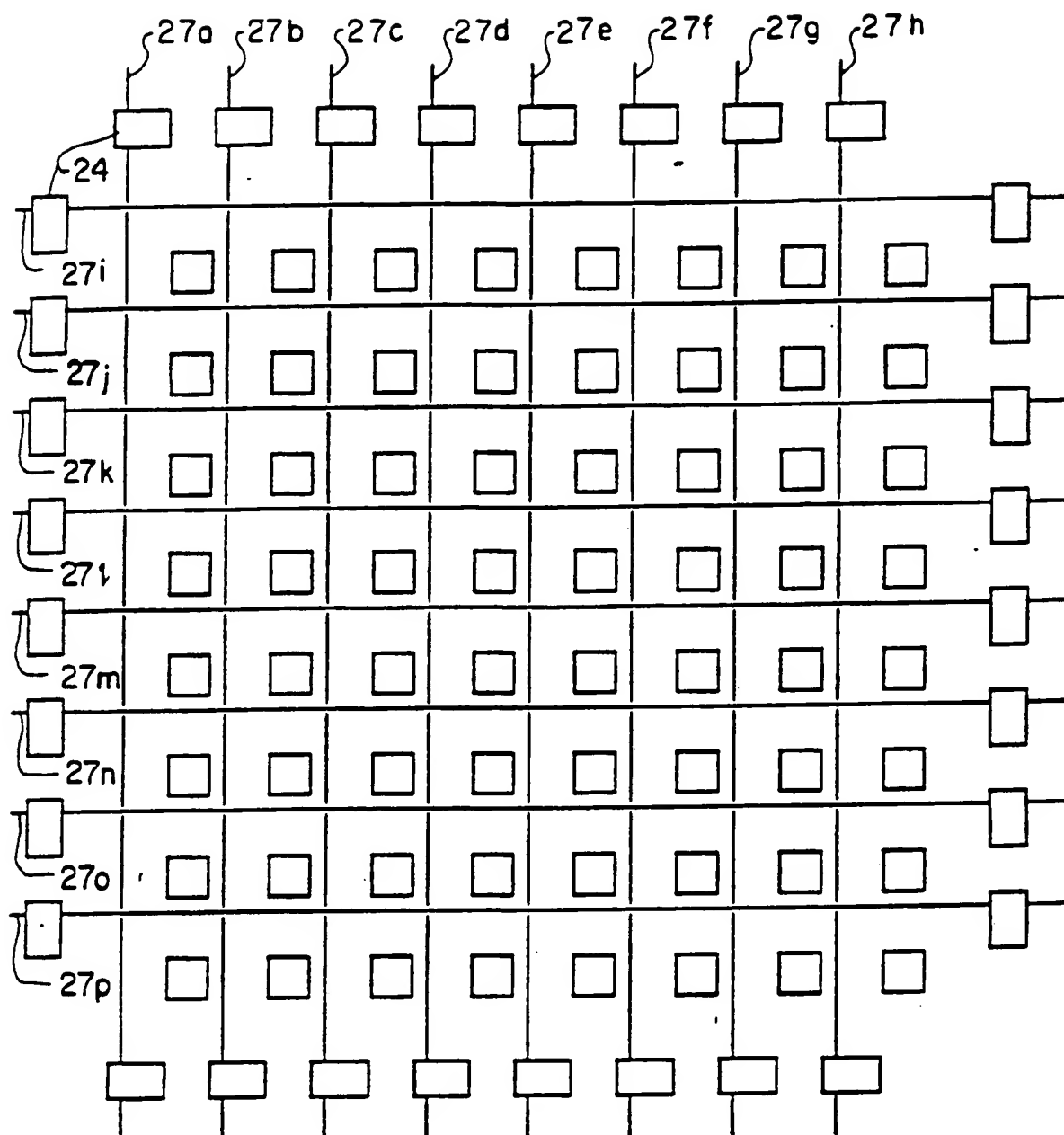
FIG. 8
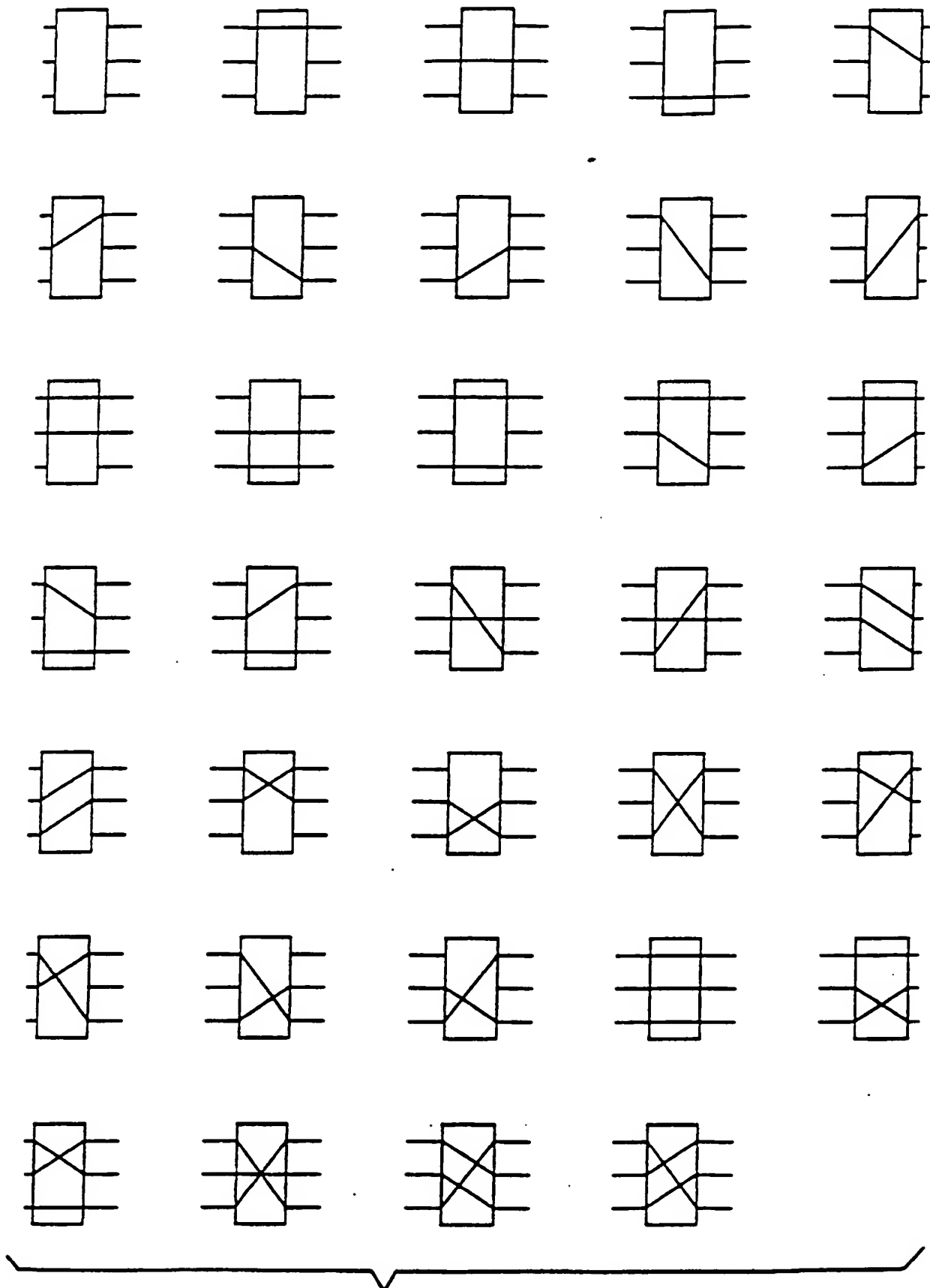
FIG. 9
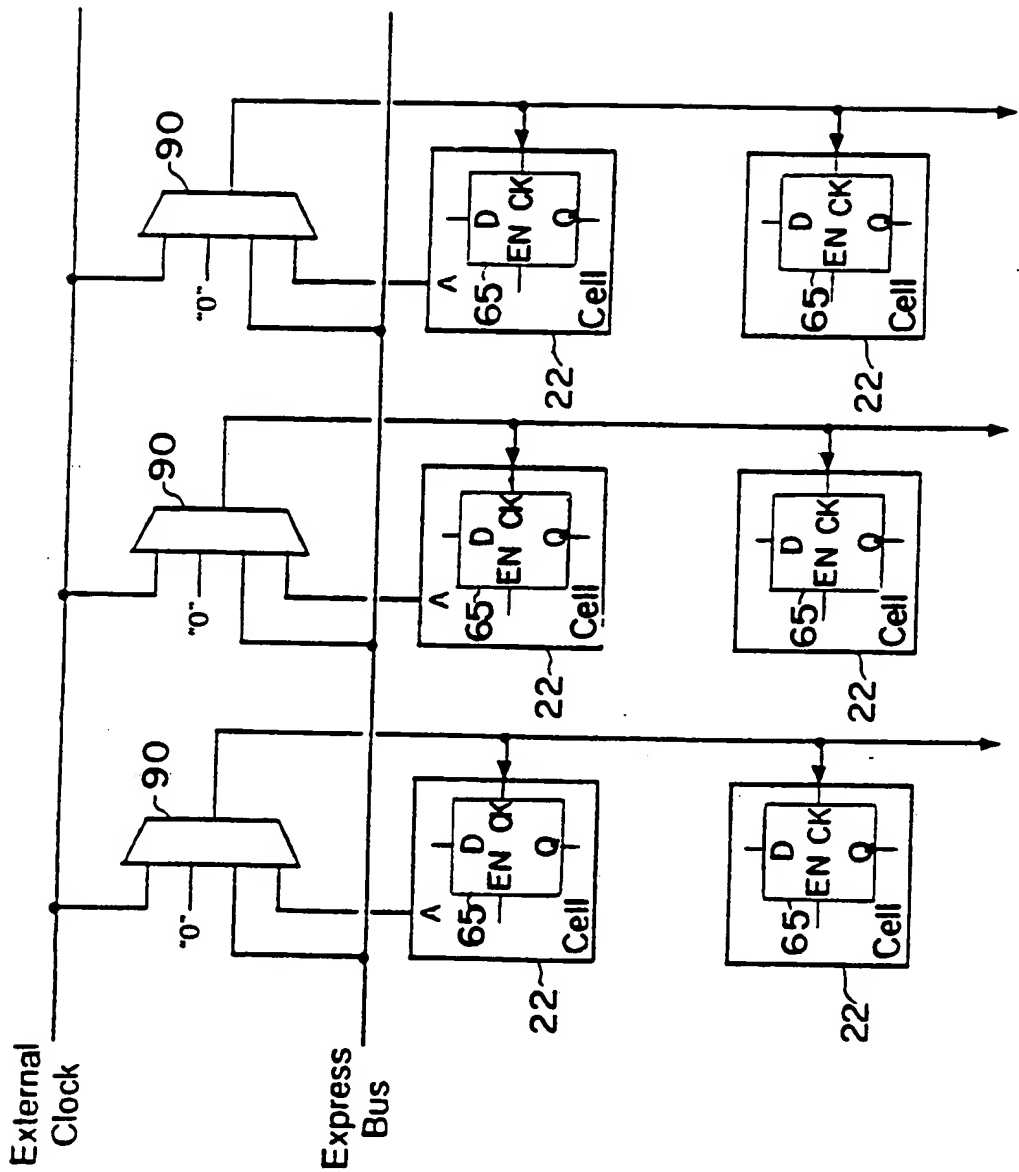
FIG. 10

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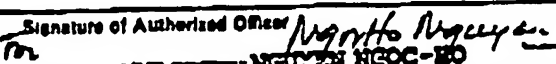
FIG. 11

INTERNATIONAL SEARCH REPORT

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL. 5   HO3K   19/177

U.S. CL.:   307/465,465.1

II. FIELDS SEARCHED

Minimum Documentation Searched

Classification System	Classification Symbols
U.S. CL.	307/465,465.1,468,469,243,303.2 340/825.83,825.87,825.91

Documentation Searched other than Minimum Documentation
to the Extent that such Documents are Included in the Fields Searched

III. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A,P	US, A, 5,019,736 FURTEK 28 MAY 1991 See fig. 1.	1-21
A	US, A, 4,642,487 CARTER 10 FEBRUARY 1987 See fig. 4a.	1-21
A,P	US, A, 5,003,200 SAKAMOTO 26 MARCH 1991 See figs 1 and 4.	1-21
A,P	US, A, 4,992,680 BENEDETTI ET AL. 12 FEBRUARY 1991 See fig.3.	1-21
A	US, A, 4,286,904 GRAHAM, III ET AL. 22 NOVEMBER 1988. See fig.2.	1-21
A	US, A, 4,918,440 FURTEK 17 APRIL 1990 See fig.1.	1-21

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the International filing date but later than the priority date claimed

"T" later document published after the International filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
20 DECEMBER 1991	03 FEB 1991

International Searching Authority	Signature of Authorized Officer
ISA/US	DAVID HUDSPETH